



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,196	03/25/2004	Brian Holscher	TRAN-P247	8666
7590	03/06/2006		EXAMINER	
WAGNER, MURABITO & HAO LLP Third Floor Two North Market Street San Jose, CA 95113			GU, SHAWN X	
			ART UNIT	PAPER NUMBER
			2189	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/810,196	HOLSCHER ET AL.
	Examiner	Art Unit
	Shawn Gu	2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 25 March 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 25 March 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date: _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Objections

1. Claims 3, 4, 12, 14, and 20 are objected to because of the following informalities:

For claims 3, 4, 12, and 20, the phrase "is used" should be replaced by "are used".

For claim 14, the word "are" should be replaced by "is".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 and 2 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As for claim 1, the specification does not provide written description for the limitation “a tracker coupled to the prefetcher”. The specification and drawings only disclose tractors within a prefetch unit (Fig 3), but does not disclose where the prefetcher is located. Fig 4 and paragraph 1 of page 11 only disclose that the tracker can notify information to a prefetcher, but do not disclose that the tracker is coupled to the prefetcher.

As for claims 1 and 2, the limitation “recognize an access to a (corresponding) plurality of cache lines” is not provided with any written description. The specification discloses “access patterns 201 show an access to cache line x, than x+1, x+2, and so on”, then referred them as “sequential accesses” (Page 9, Lines 9-10). The disclosure indicates to the Examiner that a plurality of accesses to a plurality of cache lines are recognized, instead of “an access to a plurality of cache lines”, which would imply a single access to a plurality of cache lines simultaneously. This is not supported by any written description.

Appropriate correction is required.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-4, 6, 7, 12, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, it is unclear to the Examiner if the prefetcher refers to the Prefetch Unit (Fig 1. 120) or a component within the Prefetch Unit, as the tracker coupled to the prefetcher is contained within the Prefetch Unit, not coupled to it. Therefore, the Examiner is rejecting the claim while considering the prefetcher as a component within the Prefetch Unit.

As for claims 1 and 2, it is unclear to the Examiner if “recognize an access to a plurality of cache lines” implies a single access to a plurality of cache lines simultaneously, or a plurality of accesses to a plurality of cache lines. The Examiner is rejecting the claims in view of the second interpretation. Appropriate correction is required.

As for claim 2, it is unclear to the Examiner what is meant by “a corresponding plurality of cache liens” and what the cache lines are corresponding to. Appropriate correction is required.

As for claims 4, 12, and 20, it is unclear to the Examiner what is meant by “adjacent cache lines”. Are the cache lines adjacent to in terms of physical address, or

physical proximity? The Examiner is rejecting the claims in view of the first interpretation. Appropriate correction is required.

As for claims 6 and 7, it is unclear to the Examiner which memory blocks of claim 5 is referred to by "the memory block" of the instant claim. The Examiner is rejecting the claim by interpreting "the memory block" as the "a memory block" of claim 5. Appropriate correction is required.

As for claims 2, 3, 4, 7, and 20, it is unclear to the Examiner which processor of the base claim is referred to by "the processor" of the instant claims. Claims 1 and 18 both have two instances of "a processor". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 5-11, 13- 15, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Moreno et al. [US 6,678,795 B1] (hereinafter “Moreno”).

As for claims 1, 9, and 18, Moreno teaches a request tracking data prefetch apparatus (Fig 2, combination of 204 Li, 254 Lj, 206 CCi, 256 CCj, 282 PUM Table, 284 Prefetch Engine) for a computer system (the system in Fig 2), comprising:

a processor (Fig 2, 252 Pj);

a system memory (Fig 2, 270 Memory) coupled to the processor;

a prefetch unit (Fig 2, combination of 290 PUM Engine and 256 CCj; Col 5, Lines 56-58) coupled to the system memory;

a plurality of trackers (PUM Entries; Col 4, Lines 45-57) included in the prefetch unit, wherein the trackers are respectively configured to recognize an access to a plurality of cache lines and accesses to pages of the system memory by a processor of the computer system (Col 4, Lines 45-57; Col 5, Lines 58-67; Col 7, Lines 1-7; also presented by the rows of Fig 1’s table); and

a cache memory (Fig 2, 254 Lj) coupled to the prefetch unit, wherein the prefetch unit uses a bit vector (PUM entry bits that indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) to predictively load target cache lines from the system memory into the cache memory (Col 4, Lines 58-67; Col 5, Lines 1-2) to reduce an access latency of the processor (Col 4, Lines 36-44), and wherein the target cache lines are indicated by the trackers (Col 7, Lines 4-10 and Lines 28-63).

It is clear claim 1's apparatus for a computer system is already described by the apparatus of claim 9, and the high latency memory and low latency memory of claim 1 respectively correspond to the system memory and cache memory of claim 9.

It is also clear that the method of claim 18 is performed by the apparatus of claim 9, as the bit vector of claim 9 clearly tracks a data transfer pattern (as clearly indicated by the cache line access history pattern displayed by the rows of Fig 1) between the high latency memory/system memory and the lower latency memory/cache memory.

As for claims 2 and 10, Moreno further teaches each of the trackers include a tag (PUM entry bits that indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) configured to recognize accesses to a corresponding plurality cache lines of the high latency memory by the processor.

As for claims 3 and 11, Moreno further teaches a plurality of system memory accesses by the processor to the high latency memory as recognized by the tag are used by the trackers to determine the target cache line for a predictive load into the cache memory/low latency memory (Col 7, Lines 4-10 and Lines 28-63).

As for claim 5, Moreno further teaches the high latency memory comprises a memory block of a plurality of memory blocks of the computer system (pages; Col 4, Lines 36-44).

As for claims 6 and 13, Moreno further teaches the system memory comprises a plurality of 4KB pages (Col 4, Lines 36-44; Col 5, Lines 11-14), and the memory block comprises a four kilobyte page (a memory block is a 4KB page).

As for claims 7 and 14, Moreno further teaches each of the plurality of trackers includes a tag configured to monitor a sub portion of the memory block/page for accesses by the processor (a portion of the PUM entry bits which indicate cache line accesses of a page, in other words; Col 4, Lines 45-57; Col 5, Lines 3-22; since access to every cache line of a page is represented by a corresponding bit in the PUM entry, a portion of those bits monitor a sub portion of a page for accesses).

As for claim 8, Moreno further teaches the high latency memory is a system memory (Fig 2, 270 Memory; Col 5, Lines 36-55; Memory 270 is main memory of computer system 200) of the computer system.

As for claim 15, Moreno further teaches the cache lines 128 byte cache lines (Col 5, Lines 12-14) and wherein a tag (half of the PUM entry bits which indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) is used to monitor half of a page (since access to every cache line of a page is represented by a corresponding bit in the PUM entry, half of those bits monitor half of a page) for accesses by the processor.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 4, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1].

As for claims 4, 12, and 20, Moreno further teaches accesses by the processor to adjacent cache lines of a page (Fig 1, rows with adjacent "1"s) of the system memory is used to determine the target cache line for a predictive load into the cache memory (Col 4, Lines 45-57; Col 5, Lines 3-22; Col 7, Lines 4-10 and Lines 28-63).

Moreno does not specifically teach that these accesses are consecutive. However, in Moreno's Fig 1, rows with Indexes 184772, 1502531, 1502688 all indicate 2 or 3 total page accesses to a page with only 2 adjacent cache lines indicated as accessed, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant invention that objects or programs bigger than a cache line (128 bytes) are stored in more than one adjacent cache lines of the same page, and when they are requested by the processor, these cache lines will be accessed consecutively by the processor. For instance, if an object between the size of 129 bytes and 256 bytes is

stored in the page with index 184772, then a request by the processor for this object would result in consecutive accesses to the two adjacent cache lines storing the object, and these accesses are used by Moreno's invention to determine the target cache line for a predictive load into the cache memory.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Bittel et al. [US 6,820,173 B1] (hereinafter "Bittel").

As for claim 16, Moreno already substantially discloses the claim as described above, but does not specifically disclose that the cache memory is a prefetch cache memory within the prefetch unit. However, Bittel teaches a prefetch apparatus (Fig 7) comprising a prefetch unit (Fig 3, 208 Prefetcher), and a cache memory (Fig 3, 306 Cache) within the prefetch unit. It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to include Bittel's cache memory in Moreno's prefetch unit in order to further increase caching capacity of the system while allow the existing caches (L1, L2, etc) to serve their original purposes, furthermore by using an internal cache of the prefetcher instead of the L1 cache, there is no additional interconnection wiring required between the prefetcher and the L1 cache.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Microsoft Computer Dictionary(hereinafter "Microsoft").

As for claim 17, Moreno already substantially discloses the claim as described above, and further teaches the cache memory is an L1 cache memory (Col 5, Lines 12-13), but does not specifically disclose that the cache memory is an L2 cache memory. However, Microsoft discloses that a typical L2 cache has bigger capacity than a typical L1 (Page 304), and therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make Moreno's cache memory a L2 cache instead of a L1 cache in order to have larger caching capacity.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Brooks [6,081,868] (hereinafter "Brooks").

As for claim 19, Moreno already substantially discloses the claim as described above, and further teaches the computer system includes a plurality of processors (Fig 2, 202 Pi and 252 Pj), and wherein each of the processors is coupled to a respective lower latency memory (Fig 2, 204 Li and 254 Lj) and are all coupled to a high latency memory (Fig 2, 270 Memory), but does not specifically disclose that each of the processors is coupled to a respective high latency memory. However, Brooks teaches a prefetch system wherein each of a plurality of processors is coupled to a respective

high latency memory (Brooks: Fig 2, a CPU is coupled to a CPU private memory in each CPU block; CPU Private Memory has higher latency than CPU Cache), in order to provide data storage exclusively for the associated CPU (Brooks: Col 5, Lines 25-30). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make each of Moreno's plurality of processors to be coupled to a respective high latency memory in order to provide data storage exclusively for the associated processor.

Conclusion

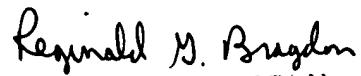
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shawn X Gu
Patent Examiner
Art Unit 2189



Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER